

SYSTEM AND METHOD FOR HEATING AND COOLING WAFER AT ACCELERATED RATES

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RELATED APPLICATIONS

[0001] This is a continuation-in-part of U.S. patent application serial no. 10/100,934 filed on March 18, 2002 and claims priority to PCT patent application serial no. _____, filed on March 18, 2003, which applications are incorporated herein in their entirety by this reference.

BACKGROUND

1. Field of the Invention

[0002] The present invention relates generally to semiconductor processing, and relates more specifically to the heating and cooling of wafers used to make integrated circuits.

2. Related art

[0003] Microelectronic devices are fabricated employing multiple layers of materials formed upon suitable carriers or substrates. Many of the layers of microelectronics materials must be patterned and registered accurately to produce fine dimensions. As circuit density and performance requirements have increased, the tolerances and dimensions of the patterns have become correspondingly smaller. It is common practice to form patterns in layers of microelectronic materials employing photolithography, wherein the layer of material to be patterned is coated with a light sensitive lacquer or photoresist material, which is then exposed to a pattern of light radiation to form the latent image of the pattern in the photoresist material. This latent image is then chemically developed to form a photoresist etch mask of the pattern, which can then be transferred to the underlying material layer by additive or subtractive processes such as etching or other analogous processes.

[0004] As feature sizes in the production of integrated circuits approach 100 nm, problems of packing density become increasingly difficult to overcome. The major problem is lithographic exposure tool resolution for exposure of photoresists. Photoresists and the manipulation of photoresists are well known in the art, but a short description of some important issues follows. Photoresists are applied as a thin film coating to a suitable substrate. Upon imagewise exposure of the coated substrate to actinic radiation, the difference in solubility rates between exposed and unexposed areas produces an image on the substrate after development. The uncovered substrate is thereafter subjected to an etching process. Frequently, this involves a plasma etching against which the resist coating must be sufficiently stable. For a positive tone photoresist, the coating protects those areas of the substrate from the etchant which were covered during the exposure, and thus the etchant is only able to etch the areas which were uncovered. The photoresist coating protects the covered areas of the substrate from the etchant and thus the etchant is only able to etch the uncovered areas of the substrate. Thus, a pattern can be created on the substrate which corresponds to the pattern of the mask or template that was used to create selective exposure patterns on the coated substrate prior to development.

[0005] The ability to reproduce very small dimensions is extremely important in the production of large scale integrated circuits on silicon chips and similar components. As the integration degree of semiconductor devices becomes higher, finer photoresist film patterns are required. One way to increase circuit density on such a chip is by increasing the resolution capabilities of the resist.

[0006] The optimally obtainable microlithographic resolution is essentially determined by the radiation wavelengths used for the selective irradiation. However, the resolution capacity that can be obtained with conventional deep UV microlithography (i.e. 248 nm) has its limits. In order to be able to sufficiently resolve optically small structural elements, e.g. features of 0.13 microns and smaller, radiation of ever shorter wavelengths (particularly 193 nm) is being employed together with a new generation of chemical amplification resist films.

[0007] A typical chemical amplification photoresist film comprises a polymer, a photoacid generator, and other optional additives. The polymer is required to be

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soluble in the chosen developer solution, and have high thermal stability and low absorbtance to the exposure wavelength in addition to having excellent etch resistance. Chemically amplified photoresists are based on chemically amplified deblocking. With this mechanism, a molecule of photogenerated acid catalyzes the breaking of bonds in a protecting group of a polymer. During the deblocking process, another molecule of the same acid is created as a byproduct, and continues the acid-catalytic deblocking cycle.

[0008] Chemically amplified resists require both an exposure dose to generate a latent acid and image and a thermal dose to drive the deblocking reaction that changes the solubility of the resist in developer. Because the photogenerated acid diffuses through the resist as it catalyzes the deblocking reaction, the acid could diffuse into unexposed regions and have a significant impact on the quality of the image generated in the resist. An important criteria of the post-exposure bake process (PEB) is optimization of the balance between the relative rates of the diffusion and reaction processes. Pre diffusion reaction processes may include photo acid loss to the environment. The post diffusion reaction processes are more specifically, the amplification reaction and the acid loss reaction. Because the diffusivity and the reaction rate are both temperature dependent, careful manipulation and monitoring of the thermal history of the resist is critical to the final dimensions of the integrated circuit. The diffusion process, the amplification reaction process, and the acid loss reaction each have different activation energies. The activation energies for diffusion and for the amplification reaction are both high, whereas the activation energy for the acid loss reaction is low in comparison.

[0009] Because of this, the ramp or rise time is critical in the formation of dense features. Lines or other features that are densely located may join together in a process known as scumming, whereas isolated lines or features exposed to the same thermal dose will increase linearly and be well resolved. At the beginning of the bake, the acid loss reaction scavenges acid before the wafer reaches a temperature that is hot enough to drive the deblocking reaction. After the hotplate temperature is reached, acid loss, diffusion and amplification occur simultaneously. Delays in reaching the bake temperature can result in substantial acid loss before deblocking can

begin, contributing to the aforementioned scumming process. For more information please refer to an article by Mark D. Smith which is hereby incorporated by reference in its entirety, entitled "Modeling the impact of thermal history during post exposure bake on the lithographic performance of chemically amplified resists," proceeding of SPIE, Vol. 4345, 1013-1021, 2001, Advances in Resist Technology and Processing XVIII.

[0010] FIGS. 1-3 illustrate a prior art oven used for post-exposure baking of silicon wafers. FIG. 1 is an exploded view of a prior art oven illustrating a top enclosure 20, gas inlet 22, showerhead 24, wafer 28, hot plate 32 with proximity pins 34, lift off pins 36 and bottom enclosure 40. FIG. 2 is a cross section of the prior art oven shown in FIG. 1 in the open position, with wafer 28 elevated from the surface of hotplate 32 and proximity pins 34. FIG. 3 is a cross section of the prior art oven shown in FIG. 1 in a closed position, with the wafer 28 upon proximity pins 34 of hot plate 32. Showerhead 24 has passages to distribute the gas arriving from gas inlet 22. One example of such an oven is manufactured by Tokyo Electron Corporation (TEC) of Kumamoto, Japan.

[0011] Generally the proximity pins raise wafer 28 about 100-150 microns off of the surface of hot plate 32. In practice, wafer 28 cannot be made or maintained during prior processing perfectly flat, and there are differences in the degree of flatness from wafer to wafer. Because of the vertical temperature gradient within the oven, even small variations in flatness can result in a relatively large disparity in the temperature at different points across wafer 28. For example, if the wafer is concave such that the ends are further from hotplate 32 than the middle, the middle portion will be hotter than the ends. This variation may result in a rise time that differs by a factor of two at different areas of the wafer in the prior art design, and is thus detrimental to precision activation and control of the diffusion and reaction processes.

SUMMARY

[0012] One aspect of the present invention is a system for varying the temperature of a wafer comprising a first temperature controlled plate. A second temperature controlled plate has proximity pins, and the wafer is located between the first and

second temperature controlled plates. The distance of the wafer from the first temperature controlled plate is maintained by proximity pins. The distance of the wafer from the second temperature controlled plate can be maintained in any number of ways but is preferably maintained by the proximity pins of the second hot plate. An enclosure surrounds the first and second temperature controlled plates and the wafer, and the enclosure comprises a gas input and output. A heat conducting gas flows from the input past the wafer and to the output.

[0013] Another aspect of the present invention involves a method of conditioning a wafer having a first and a second side within a chamber. The method comprises heating or cooling the wafer from the first side, heating or cooling the wafer from the second side, and applying a gas to the wafer, the gas distributed through a plurality of passages passing through one of the temperature control elements, such that the gas flow is controlled and is substantially laminar and spatially distributed.

[0014] Yet another aspect of the invention is a device for controlling the temperature of a wafer comprising a temperature control element, and a gas distribution system configured to distribute gas about a surface of the wafer, the gas distribution system comprising a plurality of flow paths, each of the plurality of flow paths comprising a laminar flow element. Within the device a wafer is located between the gas distribution system and the two temperature control elements.

[0015] Other aspects and advantages of the present invention will become apparent from the following descriptions and accompanying drawings

BRIEF DESCRIPTION OF THE FIGURES

[0016] The present invention may be better understood, and its numerous features and advantages made apparent by referencing the accompanying figures. For simplicity and ease of understanding, common numbering of elements within the illustrations is employed where an element is the same in different figures.

[0017] FIG. 1 is an exploded view of a prior art oven.

[0018] FIG. 2 is a cross section of the oven shown in FIG. 1.

[0019] FIG. 3 is a cross section of the oven shown in FIG. 1.

[0020] FIG. 4 is an exploded view of semiconductor processing chamber (“SPC”) 100.

[0021] FIG. 5 is a perspective view of flow channel plate 112.

[0022] FIG. 6 is a cross section of SPC 100 in an open position.

[0023] FIG. 7 is a cross section of SPC 100 in a closed position.

[0024] FIG. 8 is a cross section of SPC 100 in a closed position.

DETAILED DESCRIPTION

[0025] The following is a detailed description of illustrative embodiments of the present invention. As these embodiments of the present invention are described with reference to the aforementioned drawings, various modifications or adaptations of the methods and or specific structures described may become apparent to those skilled in the art. All such modifications, adaptations, or variations that rely upon the teachings of the present invention, and through which these teachings have advanced the art, are considered to be within the scope of the present invention. Hence, these descriptions and drawings are not to be considered in a limiting sense, as it is understood that the present invention is in no way limited to the embodiments illustrated.

[0026] FIG. 4 illustrates an exploded view of semiconductor processing chamber (“SPC”) 100. SPC 100 may be used to heat or cool a silicon wafer or other substrate in addition to supplying other process needs such as gas distribution and vapor removal. SPC 100 has many applications in the field of silicon wafer processing. One such application is in the post-exposure bake process described earlier. Other applications will be readily apparent to those skilled in the art.

[0027] Silicon wafer 126 is conditioned within upper housing 104 and lower housing 134. Although SPC 100 may be used to cool the wafer as well as heat it and condition it in other ways, it may be referred to as an oven.

[0028] Mechanical assembly 102 drives the opening and closing of SPC 100, i.e. it brings together or separates the upper housing 104 and lower housing 134 to close or open SPC 100. The rate of closure and opening of the upper housing 104 and lower housing 134 may be varied by mechanical assembly 102, and other components (not shown). Gas transport tubes 106a and 106b are attached to upper housing 104 and cover plate 110 respectively. Gas transport tubes 106 route an incoming gas used in the conditioning process to flow manifold 111 which is formed by cover plate 110 and flow channel plate 112. Gas flows through manifold 111 through upper hot (or chill) plate 124 which functions as part of a gas distribution system. The gas applied is generally nitrogen but the gas distribution system can, of course, transport any gas to wafer 126. Springs 108 compress the various components of SPC 100 while allowing freedom of movement and size variations of the various components, including wafer 126.

[0029] Wafer 126 is supported on lower hot (or chill) plate 132 by proximity pins 133. Proximity pins 133 are positioned to keep wafer 126 uniformly distanced from the upper surface of lower hot plate 132. They may be concentrically arranged or arranged in any other pattern upon the surface of lower hot plate 132 to minimize warping of the wafer during the heating, cooling, and conditioning processes. Precise positioning of the wafer 126 is critical in order to uniformly heat, cool, or otherwise condition wafer 126. Misalignment or improper distancing of wafer 126 from either lower hot plate 132 or upper hot plate 124 would subject different areas of wafer 126 to different temperature profiles or gradients. Even minimal differences in the temperature profile that a wafer may be subjected to during the conditioning process can have major effects on the line width and circuit formation of integrated circuits being formed on/in wafer 126. In the case where hot plate 132 is used to heat the wafer, it has electrical heating elements embedded within it. In the case that hot plate 132 is used as a chill plate to cool the wafer, a thermoelectric cooler or any other well known means such as cool liquid passages may be employed. Thus the term hot plate is defined as a temperature controlling plate that may either heat or cool its surroundings.

[0030] Lift pin assembly 130 is used to place wafer 126 on the proximity pins 133 when the wafer is inserted and also to lift wafer 126 from the proximity pins 133 when the wafer is removed from SPC 100.

[0031] Exhaust ring 128 restricts and controls the flow of exhaust exiting from the edge of hot plate 132 within SPC 100. Different levels of exhaust restriction can be tailored for different processing applications. Exhaust ring 128 assures uniformity of flow around the annular exhaust opening formed between exhaust ring 128 and hot plate 132. With the input and exhaust rate controlled, SPC 100 provides for radial adjustment and control of the gas flow rate over the surface of wafer 126. Distribution of the gas will now be described in further detail with regard to FIG. 5.

[0032] FIG. 5 shows flow channel plate ("FCP") 112 of manifold 111. Cover plate 110 (not shown) seals against the topside of FCP 112. Specifically, cover plate 110 makes direct contact with seal ring 113 and planar contact area 122. Alternatively, an additional gasket can be included between FCP 112 and cover plate 110. Gas arrives from gas transport tubes 106 through cover plate 110 into an annular channel formed by distribution ring 114, which is a recessed portion of FCP 112, and cover plate 110. FCP 112 is preferably formed by etching a piece of metal, or metal foil, although many other well known metal-working methods may be employed. Alternatively, cover plate 110 may be formed to provide the gas distribution ring. Additionally, although a metal such as nickel or stainless steel is preferred in order to avoid contamination of the wafer, any other material known in the art may be employed to form manifold 111. Distribution ring 114 is recessed relative to seal ring 113. Gas flows through the annular channel above distribution ring 114 through various distribution channels 116 to different areas of the surface of wafer 126 (not shown). Annular channel 114 ranges from 2mm to 2cm in width and from 0.2mm to 5mm in depth. Distribution channels 116 each have a feed passage 117 and a laminar flow passage ("LFP") 118. The laminar flow passages 118 assure constant and evenly distributed flow upon the surface of the wafer. The LFPs 118 are tailored to optimize the flow distribution for a range of applications. Generally speaking, the depth of distribution channels 116 may range from about 50 microns to about 800 microns and is preferably 150 microns. For more information on laminar flow passages please

refer to U.S. Patent No. 4,685,331 to Renken et al., entitled "Thermal Mass Flow Meter and Controller," which is hereby incorporated by this reference in its entirety. Feed passages 117 transport the gas from distribution ring 114 to LFPs 118. At the end of each distribution channel is gas delivery cavity 120. Each gas delivery cavity 120 is aligned with a gas passage through upper hot plate 124.

[0033] Any solvents or contaminants that are present within SPC 100, for instance those that may originate or evaporate from wafer 126 during the post-exposure bake and travel through the passages in upper hot plate 124, will condense and/or accumulate in gas delivery cavities 120. Thus, gas delivery cavities 120, which are fabricated to a much greater depth than the laminar flow passages to accommodate condensed contaminants, protect laminar flow passages 118 from contaminants and any resultant clogging or flow impediment.

[0034] FCP 112 is in direct contact and in close proximity with upper hot plate 124. Thus, FCP 112 is at nearly the same temperature as upper hot plate 124. Depending on whether the upper hot (chill) plate is acting to heat or cool the wafer, the gas flowing through manifold 111 will be heated or cooled to roughly the same temperature as the wafer. Furthermore, the gas also passes directly through passages in upper hot plate 124, thus further assuring that the gas temperature arrives at a temperature of SPC 100 very near to the temperature at or near the surface of wafer 126. Because of the large temperature controlled surface area used for gas transport, the relatively long presence time of the gas in contact with temperature controlled elements, and the direct passage of the gas through the temperature controlled elements, heat is efficiently transferred to the gas. In the fabrication of very small integrated circuits having, for example, line widths of 0.18 microns and smaller, this is a distinct advantage over the prior art, because the precise control of the temperature at the surface of the wafer directly impacts the relative rates of the diffusion and reaction processes, and thus the line width of the integrated circuits.

[0035] FIGS. 6-8 are cross sections of SPC 100 in various stages of operation. FIG. 6 shows SPC 100 open with wafer 126 in an elevated position. Wafer 126 is inserted onto lift pin assembly 130, which is in the up position. In FIG. 7, lift pin assembly 130 has lowered wafer 126 onto proximity pins 133 on lower hot plate 132.

Upper hot plate 124 is in an up position as are flow channel plate 112 and cover plate 110 of manifold 111. One or both of hot (chill) plates 124 and 134 may be active in this stage in order to heat or cool wafer 126. In addition, the gas may be flowing or may be turned off. Note the gap between the upper hot plate 124 and wafer 126.

[0036] In FIG. 8, upper hot plate 124 has been lowered to the down position such that upper proximity pins 125 are in contact with lower hot plate 132. The temperature of wafer 126 may be controlled in many ways, and the temperature gradient within SPC 100 may also be adjusted by modulating hot plates 124 and 132 together or independently. The rate of movement (lowering or lifting) of the upper and lower hot plates may be varied by the system during operation in order to modulate the temperature profile. This may be controlled in conjunction with the opening and closing of the enclosure for complete control of the time/temperature profile of the wafer. By activating both the upper hot plate 124 and the lower hot plate 132, the gradient in SPC 100 is greatly minimized compared to prior art designs only having a lower hotplate. Furthermore, with the use of extending upper proximity pins 125, the distance between the upper and lower hot plates can be altered in process to provide maximum flexibility and adjustability to the temperature profile. The temperature schedules of the hot plates can also be programmed to individually vary with time during any given temperature cycle or profile. Generally speaking, the ramp time to a given temperature can be cut in half with the dual hot plate design of the current invention, in comparison the prior art designs. The ramp rate can also be much more precisely controlled compared to prior designs.

[0037] Furthermore, because the heat is applied to the wafer from both sides, flatness variations (warping) are better accommodated than with prior designs such as that of FIGS. 1-3. For example, if the wafer is warped such that the ends of the wafer are further from the lower hot plate 132 than the center portion of the wafer, those same ends will be nearer to upper hot plate 124. The warp of a 200mm wafer can be up to about 75 microns. In other words, the reduced heat gradient between the lower and upper hot plates 124 and 132 minimizes the temperature difference that imperfect wafers would otherwise be subjected to. This, in turn, leads to more precise integrated circuit formation.

[0038] Gas can be applied to the wafer with upper hot plate 124 in the up or down position as seen in FIGS. 7 and 8. Also, in the cross sections of FIGS. 6-8, the gas passages 127 through upper hot plate 124 may be seen. As the gas flows through manifold 111 and gas passages 127 it is heated to the temperature of the upper hot plate 124. As mentioned previously, the temperature of upper hot plate 124 may be independently manipulated. Thus, the temperature of the gas distributed may also be heated or cooled to be at a selected temperature in order to produce a desired effect. The relatively long residual time of the gas and the large surface area of the heat transfer elements increases the precision temperature control of the gas, and thus the wafer, in comparison with prior art designs. In addition the control afforded by the laminar flow channels that are dispersed to provide even flow about the surface of the wafer yields better control of the temperature within SPC 100.

[0039] The precise temperature control and fast dynamic response of SPC 100 are assets in many operations. In particular, SPC 100 can better control the important transitions of chemically amplified resists. As mentioned previously, chemically amplified resists require differing thermal profiles and energies to activate diffusion, the amplification reaction, and the acid loss reaction. Thus, precise temperature control is of the utmost importance so that any reaction is not inadvertently started or affected. Because the photogenerated acid diffuses through the resist as it catalyzes the deblocking reaction, the acid may otherwise diffuse into unexposed regions and have a significant impact on the quality of the image generated in the resist. An important criteria of the post-exposure bake process (PEB) is optimization of the balance between the relative rates of the diffusion and reaction processes. Because the diffusivity and the reaction rate are both temperature dependent, careful manipulation and monitoring of the thermal history of the resist is critical to the final dimensions of the integrated circuit. The dual heating and cooling system and the precision gas distribution system of the present invention make this possible.

[0040] While embodiments of the present invention have been shown and described, changes and modifications to these illustrative embodiments can be made without departing from the present invention in its broader aspects. Thus, it should be evident that there are other embodiments of this invention which, while not expressly

described above, are within the scope of the present invention. Therefore, it will be understood that the appended claims necessarily encompass all such changes and modifications as fall within the described invention's true scope; and further that this scope is not limited merely to the illustrative embodiments presented to demonstrate that scope.